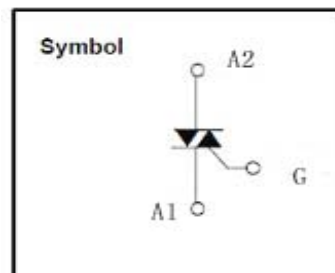


Features

- Repetitive Peak off-State Voltage: 600V
- R.M.S On-State Current($I_{T(RMS)}=1A$)
- Low on-state voltage: $V_{TM}=1.2(\text{typ.})@ I_{TM}$
- Low reverse and forward blocking current:
 $I_{DRM}=500\mu A@TC=125^{\circ}C$
- Low holding current: $I_H=4mA$ (typ.)
- High Commutation dV/dt .



General Description

General purpose switching and phase control applications.

These devices are intended to be interfaced directly to micro-controllers, logic integrated circuits and other low power gate trigger circuits such as fan speed and temperature modulation control, lighting control and static switching relay.



Absolute Maximum Ratings ($T_J=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DRM}	Peak Repetitive Forward Blocking Voltage(gate open) (Note 1)	600	V
$T_{(RMS)}$	Forward Current RMS (All Conduction Angles, $T_L=50^{\circ}C$)	1	A
I_{TSM}	Peak Forward Surge Current, (full Cycle, Sine Wave, 50/60 Hz)	9.1/10	A
I^2t	Circuit Fusing Considerations ($t_p=10$ ms)	0.41	A^2s
P_{GM}	Peak Gate Power — Forward, ($T_c=58^{\circ}C$, Pulse with $\leq 1.0\mu s$)	5	W
$P_{G(AV)}$	Average Gate Power — Forward, (Over any 20ms period)	0.1	W
dI/dt	Critical rate of rise of on-state current $I_{TM}=1.5A$; $I_G=200mA$; $dI_G/dt=200mA/\mu s$ $T_J=125^{\circ}C$	50	$A/\mu s$
I_{FGM}	Peak Gate Current — Forward, $T_J=125^{\circ}C$ (20 μs , 120 PPS)	0.5	A
V_{RGM}	Peak Gate Voltage — Reverse, $T_J=125^{\circ}C$ (20 μs , 120 PPS)	6	V
T_{Ji}	Junction Temperature	-40~125	$^{\circ}C$
T_{stg}	Storage Temperature	-40~150	$^{\circ}C$
	mass	2	g

Note1: Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on-state. The rate of rise of current should not exceed $3A/\mu s$.

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	60	$^{\circ}C/W$
R_{QJA}	Thermal Resistance, Junction-to-Ambient	-	-	120	$^{\circ}C/W$

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Characteristics	Min	Typ.	Max	Unit	
I _{DRM}	Peak Forward or Reverse Blocking Current (V _D = V _{DRM} /V _{RRM} , gate open)	-	-	5	μA	
		-	-	500		
V _{TM}	Forward "On" Voltage (I _{TM} = 1.5 A)	-	1.2	1.5	V	
			(Note2)			
I _{GT}	Gate Trigger Current (Continuous dc) (V _D = 12 Vdc, R _L = 33 Ω)	-	0.4	5	mA	
		-	1.3	5		
		-	1.4	5		
		-	3.8	7		
V _{GT}	Gate Trigger Voltage (Continuous dc) (V _D = 12 Vdc, R _L = 33 Ω)	-	-	1.2	V	
		-	-	1.2		
		-	-	1.2		
		-	-	1.5		
V _{GD}	Gate threshold voltage(T _J =125°C, V _D =V _{DRM} , R _L =3.3KΩ)	0.2	-	-	V	
dV/dt	Critical rate of rise of commutation Voltage (V _D =0.67V _{DRM} , gate open)	10	20	-	V/μs	
I _H	Holding Current (V _D = 12 V, I _{GT} = 100 mA)	-	1.3	5	mA	
I _L	latching current (V _D = 12 V; I _{GT} = 100 mA)	T2+G+	-	1.2	5	mA
		T2+G-	-	4.0	8	
		T2-G-	-	1.0	5	
		T2-G+	-	2.5	8	
R _d	Dynamic resistance (T _J =125°C)	-	-	420	mΩ	

Note 2. Forward current applied for 1 ms maximum duration, duty cycle

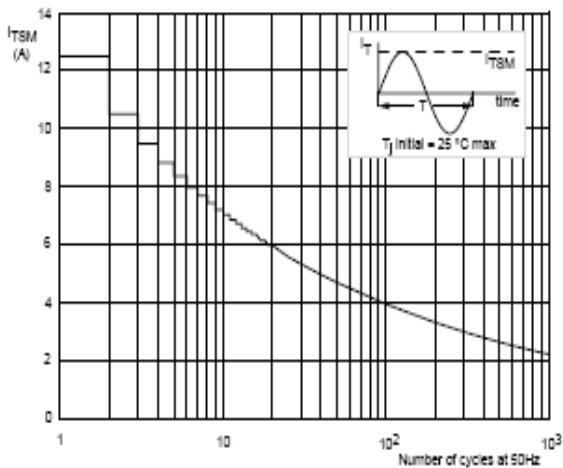


Fig. 1 Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

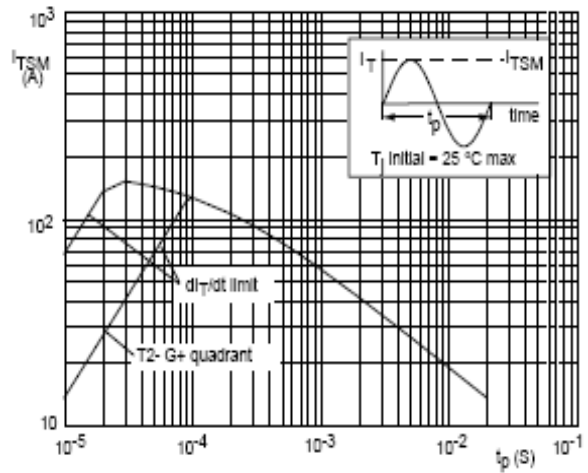


Fig. 2 Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20$ ms.

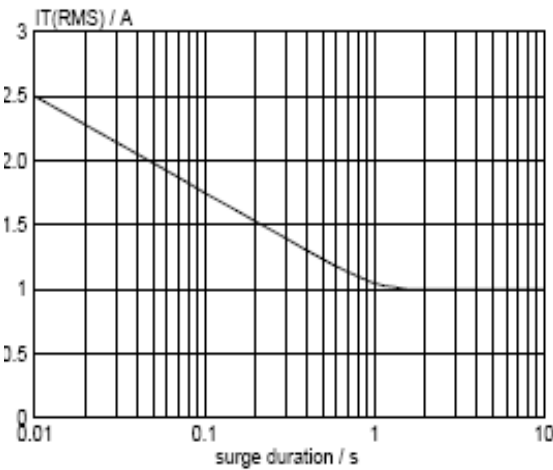


Fig. 3 Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{lead} \leq 66^\circ\text{C}$.

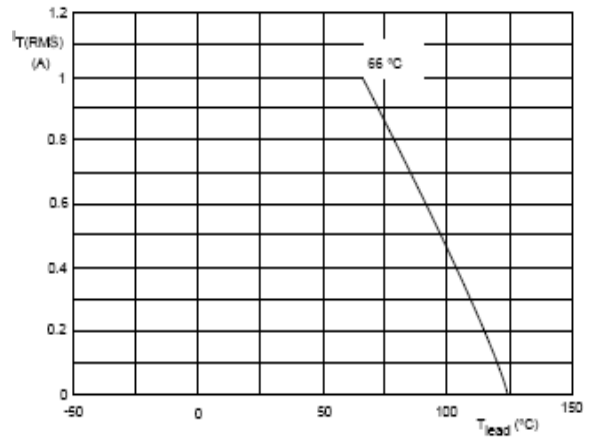


Fig. 4 Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead} .

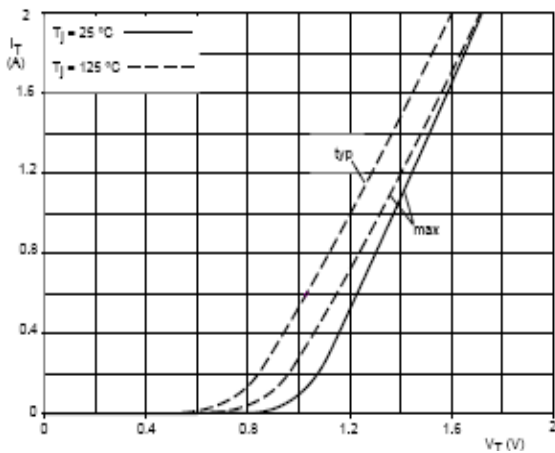


Fig. 5 Typical and maximum on-state characteristic.

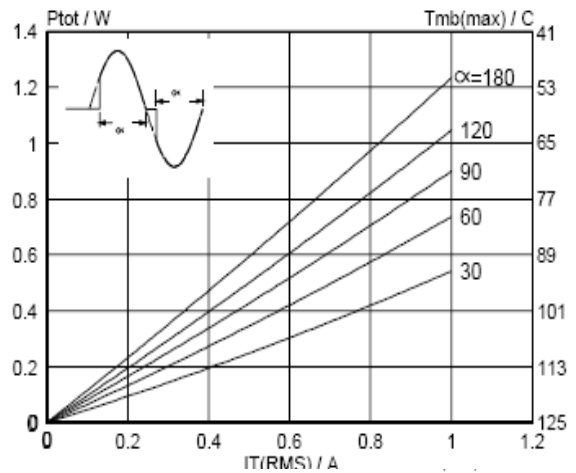


Fig. 6 Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where $\alpha =$ conduction angle.

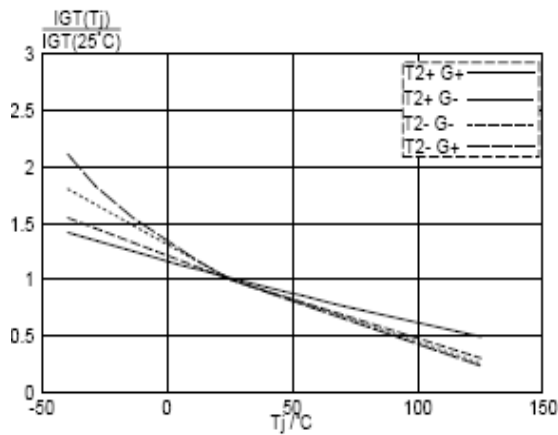


Fig. 7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

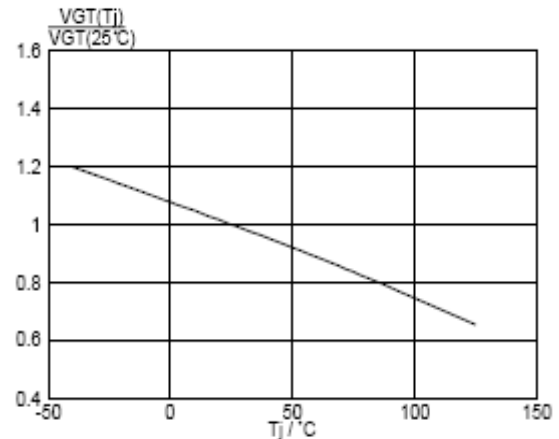


Fig. 8. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

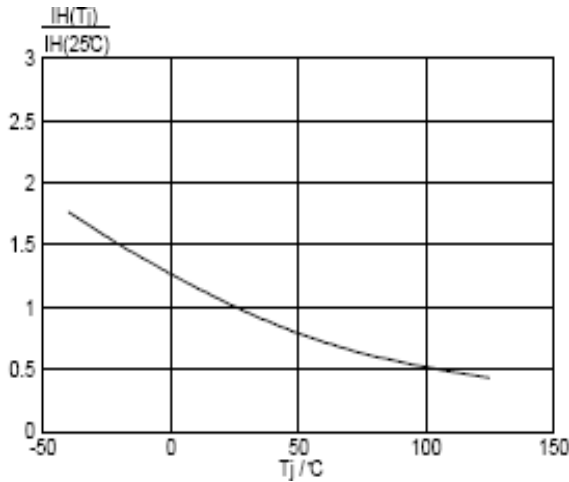


Fig. 9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j .

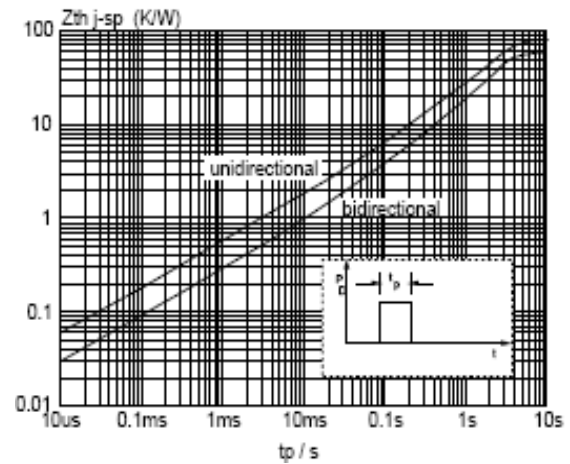


Fig. 10 Transient thermal impedance $Z_{th(j-sp)}$, versus pulse width t_p .

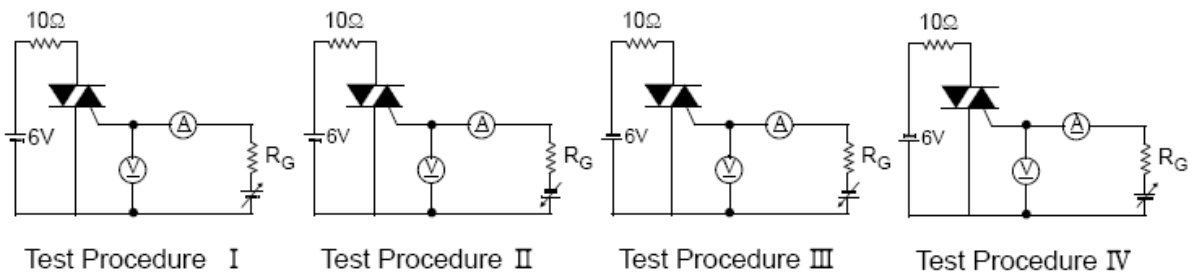


Fig. 11 Gate Trigger Characteristics Test Circuit

TO-92 Package Dimension

